



Open-Source Process Design Kits Could Change How Universities Teach Chip Design

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Abstract

A process design kit is the set of device models, layout rules, cell libraries and verification decks that connects a circuit designer to a particular fabrication line. For decades universities have obtained such kits only under non-disclosure agreements, and the terms of those agreements have quietly shaped what is taught: students cannot publish their layouts, cannot take their work with them and often cannot be shown the rules they are designing to. Since 2020 several foundries have released manufacturable kits under open licences, and a complete open-source tool flow now exists to use them. This perspective argues that the change matters for teaching more than for research. An open kit lets a course cover the whole path from description to verified layout on a real process, lets instructors share complete worked designs, and lets students inspect the device models and rule decks that proprietary flows conceal. The article also takes the objections seriously: the open processes are mature nodes far from the leading edge, the open tools lag commercial ones, employers hire for experience with commercial flows, and fabrication access depends on funding that may not last. It concludes that open kits are best used as the foundation of a curriculum, with commercial tools and advanced nodes introduced afterwards.

Keywords: *Process design kit, Open-source hardware, VLSI education, Electronic design automation, Integrated circuit design, Semiconductor workforce*

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1. Introduction

Anyone who has taught an integrated circuit design course knows the paperwork that precedes the first lecture. The foundry's kit arrives under a non-disclosure agreement signed by the institution. It may be installed only on designated machines, and students must be registered before they see it. Layouts may not appear in a thesis without clearance. Screenshots in a set of lecture slides are a grey area, and placing the course material on a public repository is out of the question. None of this is unreasonable from the foundry's side, since a process design kit (PDK) encodes hard-won knowledge of a manufacturing process, but its cumulative effect on teaching is large and seldom discussed.

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In 2020 a 130 nm CMOS process from SkyWater Technology became the first for which a foundry-backed, manufacturable PDK was published under an open licence, in a collaboration with Google (Edwards, 2020). A 180 nm kit from GlobalFoundries followed in 2022, and IHP in Germany has since opened a 130 nm BiCMOS process. Alongside them an open-source tool flow able to take a design from hardware description to mask layout has matured (Ajayi et al., 2019; Shalan and Edwards, 2020). This article argues that these developments could change the way universities teach chip design, considers the reasons for doubt, and suggests how a department might respond.

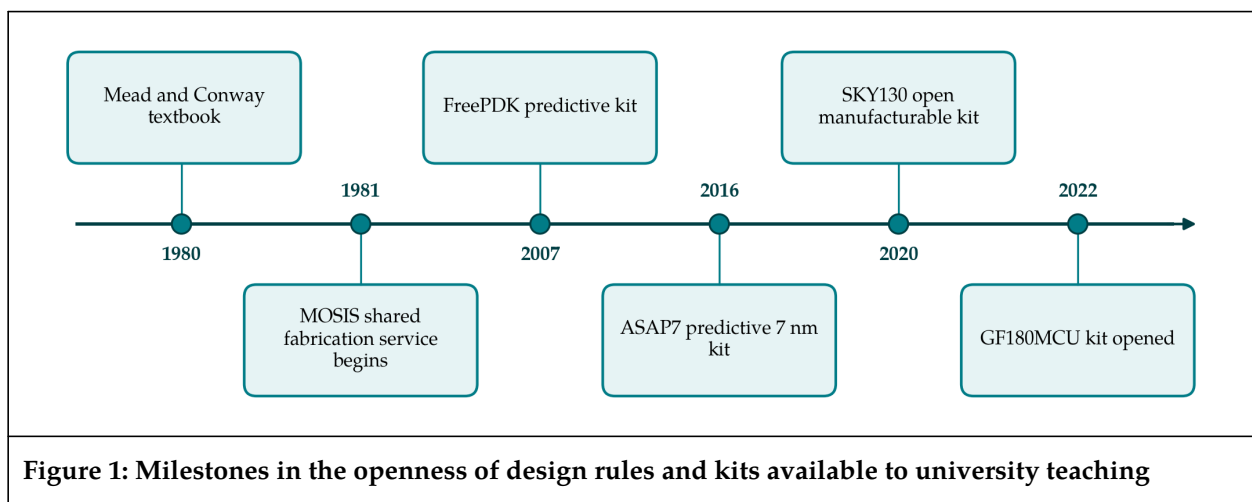
2. How Teaching Came to Sit Behind Agreements

Chip design was not always taught this way. The textbook of Mead and Conway (1980) deliberately separated design from fabrication. It gave students a set of simplified, scalable layout rules that were independent of any one manufacturer, and courses built on it spread quickly through universities, as Conway (2012) later recounted. The MOSIS service then gathered student and research designs onto shared wafers so that the cost of a fabrication run was divided among many users (Tomovich, 1988). The rules students worked with were public, and a layout could be printed in a textbook.

That openness did not survive the growing complexity of the processes. As feature sizes fell, simple scalable rules gave way to long foundry-specific rule decks, and device models became detailed descriptions of a proprietary technology. Foundries protected both by contract. Universities continued to gain access through MOSIS and its counterparts elsewhere, but as licensees. The teaching community responded with predictive kits that describe a plausible process and correspond to no real one: FreePDK for a 45 nm generation (Stine et al., 2007) and ASAP7 for a 7 nm FinFET generation (Clark et al., 2016). These can be shared freely, and they remain valuable, but nothing designed with them can be manufactured. Figure 1 places these developments in sequence.

3. What an Open Kit Changes in the Classroom

The central claim of this article is that an open, manufacturable PDK removes constraints that instructors have worked around for so long that they no longer notice them. Table 1 contrasts the two situations. The differences fall under four heads: completeness, inspectability, portability and the possibility of silicon.



Completeness comes first. With an open kit and the OpenROAD-based flow, a student can take a small processor core from register-transfer description through synthesis with Yosys (Wolf and Glaser, 2013), placement, clock tree construction, routing and sign-off checks, on a laptop, in the span of a laboratory course. Memory blocks can be generated with OpenRAM (Guthaus et al., 2016). Custom layout and extraction use Magic, a tool whose origins lie in university teaching (Ousterhout et al., 1984), and circuit simulation uses descendants of the original SPICE (Nagel and Pederson, 1973). Many courses stop at simulation or at a field-programmable gate array because the rest of the path is too awkward to provision. That reason weakens.

Table 1: Teaching conditions under a restricted commercial kit and under an open kit		
Aspect of teaching	Kit under non-disclosure agreement	Open kit
Access	Registered students on controlled machines	Anyone, on a personal laptop
Course material	Layouts and rule details cannot be published	Complete worked designs can be shared
Device models and rules	Often encrypted or summarised	Readable source files
Student portfolio	Work stays inside the institution	Designs can be shown to employers
Reproducibility	Published results cannot be rebuilt by others	Design, kit and tools can be archived together
Process node	Access possible to advanced nodes	Mature nodes only
Tool maturity	Production-proven commercial flows	Open flows, less capable and less supported

Inspectability is the second head, and it bears most on analog and device teaching. Textbooks explain design with simplified transistor equations and then warn that real devices behave differently (Razavi, 2017). In a commercial kit the model files that embody the difference are frequently encrypted. In an open kit a student can read the model cards, plot the characteristics of every device the process offers, and see how a design rule relates to the layers it constrains. The textbook treatment of layout rules and their physical origin (Weste and Harris, 2011) can be set beside a real rule deck instead of an idealised one.

Portability concerns what happens to the work afterwards. A design made with an open kit belongs to the student in a practical sense: it can be placed in a public repository, examined by a prospective employer, extended by the next cohort and cited by a researcher who wishes to reproduce it. Instructors can exchange complete laboratory exercises, including reference layouts, in the way that programming courses exchange code. The parallel with the open RISC-V instruction set, whose proponents made the same argument for processor architecture (Asanović and Patterson, 2014), is close.

The fourth is silicon. Multi-project shuttles on the open processes have allowed student designs to be fabricated and returned as packaged parts, and community schemes that pool very small designs onto a shared die have lowered the cost of entry further. Measuring a chip of one's own design teaches things that no simulation does, among them that the first version rarely works as intended.

4. Reasons for Doubt

The case can be overstated, and four objections deserve a direct answer. The first is that the open processes are old. A 130 nm planar technology has none of the features that occupy designers at the leading edge: no fin or nanosheet devices, no multiple patterning, no restrictive unidirectional routing. A graduate who has only seen such a process will find much that is unfamiliar in industry. This is true, and it argues for teaching the principles on an open mature node and the particular difficulties of advanced nodes with a predictive kit such as ASAP7. It does not argue for teaching neither in the open.

The second objection concerns tools. Commercial design automation is the product of decades of investment, and the open flow is behind it in quality of results, capacity and above all in analog and mixed-signal verification. Kahng (2020) asks plainly who will use and sustain open tools once they are built. For teaching, a tool that exposes its algorithms and can be modified has pedagogical value that partly offsets lower performance. Students nevertheless need to know that production practice differs.

Third, employers recruit for experience with commercial flows, and established laboratory courses are built around them. A department that replaced them wholesale would do its graduates a disservice. The fourth objection is sustainability. Fabrication runs on the open processes have relied to a considerable

degree on corporate sponsorship, and sponsorship can be withdrawn. Model accuracy and kit maintenance likewise depend on a small number of committed people. A curriculum should be designed so that it still works if free fabrication disappears, with silicon as an enrichment and the open design flow as the core.

5. Implications for Departments and Funders

If the argument holds, the sensible response is a layered curriculum. Introductory and intermediate courses would use an open kit and open tools throughout, so that every student completes at least one design to verified layout and can keep it. Advanced courses would add a commercial flow under the usual agreements and a predictive advanced-node kit, with the open flow as the common reference against which the differences are explained. Analog courses would use the open device models for the transparency they offer, and would set hand analysis, simulation and layout of the same circuit side by side.

Public funders have a part. The European Chips Act ([European Union, 2023](#)) and the United States CHIPS and Science Act ([United States Congress, 2022](#)) both treat the shortage of trained designers as a matter of policy. Regular educational shuttle runs on open processes, maintenance of the kits and the open tools, and shared course material are modest items beside the cost of a fabrication plant, and they address the same shortage from the other end. Open kits also widen who can take part: an institution with no foundry relationship and no licence budget can teach the same course as one with both.

The claim made here is conditional. Whether students taught on open kits become better designers, or reach competence sooner, is an empirical question on which systematic evidence has not yet been gathered. Departments that adopt the approach are well placed to gather it, by recording what students complete, what they retain and how they fare when they later meet a commercial flow.

6. Conclusion

For forty years the practical conditions of teaching chip design have been set by agreements written to protect process technology, not to serve education. Open process design kits lift those conditions for a class of mature processes. They allow a full design flow to be taught, examined, shared and occasionally fabricated without restriction, and they return to the classroom something of the openness of the Mead and Conway period. They do not replace commercial tools or advanced nodes in the training of a designer. Used as the foundation on which those are later introduced, they could make chip design a subject that many more universities are able to teach well.

Conflict of interest

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References

- Ajayi, T., Chhabria, V.A., Fogaça, M., Hashemi, S., Hosny, A., Kahng, A.B. et al. (2019). [Toward an open-source digital flow: First learnings from the OpenROAD project. *Proceedings of the 56th Annual Design Automation Conference*](#). <https://doi.org/10.1145/3316781.3326334>
- Asanović, K. and Patterson, D.A. (2014). [Instruction sets should be free: The case for RISC-V](#). Technical Report UCB/EECS-2014-146, University of California, Berkeley.
- Clark, L.T., Vashishtha, V., Shifren, L., Gujja, A., Sinha, S., Cline, B., Ramamurthy, C. and Yeric, G. (2016). [ASAP7: A 7-nm finFET predictive process design kit. *Microelectronics Journal*](#), 53: 105-115. <https://doi.org/10.1016/j.mejo.2016.04.006>
- Conway, L. (2012). [Reminiscences of the VLSI revolution: How a series of failures triggered a paradigm](#)

- shift in digital design. *IEEE Solid-State Circuits Magazine*, 4(4): 8-31.
<https://doi.org/10.1109/MSSC.2012.2215752>
- Edwards, R.T. (2020). Google/SkyWater and the promise of the open PDK. *Workshop on Open-Source EDA Technology (WOSET)*.
- European Union (2023). Regulation (EU) 2023/1781 of the European Parliament and of the Council establishing a framework of measures for strengthening Europe's semiconductor ecosystem (Chips Act). Official Journal of the European Union, L 229.
- Guthaus, M.R., Stine, J.E., Ataei, S., Chen, B., Wu, B. and Sarwar, M. (2016). OpenRAM: An open-source memory compiler. *Proceedings of the 35th International Conference on Computer-Aided Design*.
<https://doi.org/10.1145/2966986.2980098>
- Kahng, A.B. (2020). Open-source EDA: If we build it, who will come? *Proceedings of the 28th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*.
- Mead, C. and Conway, L. (1980). *Introduction to VLSI Systems*. Addison-Wesley, Reading, MA.
- Nagel, L.W. and Pederson, D.O. (1973). SPICE (Simulation Program with Integrated Circuit Emphasis). Memorandum No. ERL-M382, Electronics Research Laboratory, University of California, Berkeley.
- Ousterhout, J.K., Hamachi, G.T., Mayo, R.N., Scott, W.S. and Taylor, G.S. (1984). Magic: A VLSI layout system. *Proceedings of the 21st Design Automation Conference*, 152-159.
<https://doi.org/10.1109/DAC.1984.1585789>
- Razavi, B. (2017). *Design of Analog CMOS Integrated Circuits*, 2nd edition. McGraw-Hill Education, New York.
- Shalan, M. and Edwards, T. (2020). Building OpenLANE: A 130nm OpenROAD-based tapeout-proven flow. *Proceedings of the 39th International Conference on Computer-Aided Design*.
<https://doi.org/10.1145/3400302.3415735>
- Stine, J.E., Castellanos, I., Wood, M., Henson, J., Love, F., Davis, W.R. et al. (2007). FreePDK: An open-source variation-aware design kit. *Proceedings of the IEEE International Conference on Microelectronic Systems Education*, 173-174. <https://doi.org/10.1109/MSE.2007.44>
- Tomovich, C. (1988). MOSIS: A gateway to silicon. *IEEE Circuits and Devices Magazine*, 4(2): 22-23.
- United States Congress (2022). CHIPS and Science Act. Public Law 117-167.
- Weste, N.H.E. and Harris, D.M. (2011). *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th edition. Addison-Wesley, Boston.
- Wolf, C. and Glaser, J. (2013). Yosys: A free Verilog synthesis suite. *Proceedings of the 21st Austrian Workshop on Microelectronics (Austrochip)*.